

oxide regions or mesa structures) in several semiconductor materials systems. However, the present hypothesis is distinctly different (because the SiGe is engulfed in a crystalline material)"

The Examiner's reference to col. 4, ln. 16-19 of Selvakumar appears to refer to an interface between silicon-dioxide and a SiGe *channel*. The text does not specifically refer to an interface with a region of SiGe. It appears that Selvakumar has defined the SiGe *channel* to include the broader category of a small SiGe region engulfed in silicon. The SiGe *channel* will therefore have an interface with silicon-dioxide, even though the actual SiGe is separated from the silicon-dioxide by a layer of silicon as explicitly outlined in col. 5, ln. 32-42 excerpted above.

Figures 5-7, as referenced by the Examiner, indicate a "Ge implant area 8" (col. 3, ln. 47). Again, this text does not specifically refer to the SiGe region. The implant area 8 appears to be more broadly defined to include a small SiGe region engulfed in silicon. The explicit text of col. 5, ln. 32-42 appears to be the most accurate discussion in Selvakumar with respect to the interfaces involved.

The SiGe region of Selvakumar therefore is adjoined to a silicon region which in turn is adjoined to a SiO_2 gate oxide. Selvakumar does not show a $\text{Si}_{1-x}\text{Ge}_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and **wherein the $\text{Si}_{1-x}\text{Ge}_x$ channel region forms a $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$ gate oxide interface**.

In contrast, all independent claims of Applicant's invention include a $\text{Si}_{1-x}\text{Ge}_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and **wherein the $\text{Si}_{1-x}\text{Ge}_x$ channel region forms a $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$ gate oxide interface**. Applicant notes the importance of Applicant's novel implantation process through the gate oxide that allows the formation of a device including a $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$ gate oxide interface.

Because Selvakumar does not show the $\text{Si}_{1-x}\text{Ge}_x$ channel region described above, and in fact teaches away from Applicant's channel region, a 35 USC § 102(b) is not supported by Selvakumar. Reconsideration and withdrawal of Examiner's 35 USC § 102(b) rejection is therefore respectfully requested with respect to independent claims 11, 24, 25, 28, 38, 40, and 41 and all claims that depend therefrom.

§103 Rejection of the Claims

Claims 13, 26, 27, 39, 42, and 43 were rejected under 35 USC § 103(a) as being unpatentable over Selvakumar et al. (U.S. Patent No. 5,426,069) together with Crabbe' et al (U.S. Patent No. 5,821,577).

Crabbe appears to show a transistor containing a silicon germanium channel 18. However, the silicon germanium layer in Crabbe is “sandwiched between layers of pure silicon” (Col. 4, ln. 45-48). As further discussed in col. 6, ln. 22-28, a silicon cap layer 20 is deposited on the SiGe channel layer 18, and a gate insulator layer 22 is formed on the cap layer 20. Crabbe does not show or suggest a $\text{Si}_{1-x}\text{Ge}_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and **wherein the $\text{Si}_{1-x}\text{Ge}_x$ channel region forms a $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$ gate oxide interface.**

In contrast, all independent claims of Applicant's invention include a $\text{Si}_{1-x}\text{Ge}_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and **wherein the $\text{Si}_{1-x}\text{Ge}_x$ channel region forms a $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$ gate oxide interface.**

Because Crabbe fails to cure the deficiencies of Selvakumar, a 35 USC § 103 is not supported by the listed references. Reconsideration and withdrawal of Examiner's 35 USC § 103(a) rejection is therefore respectfully requested with respect to claims 13, 26, 27, 39, 42, and 43.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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Title: SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 7 day of September, 2001.

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